

## Implementing Basic Amplification Stages with Small Signal Bipolar Junction Transistors

Nicholas Perosino, Product Development Engineer

### Introduction:

Central Semiconductor boasts one of the largest small signal bipolar junction transistor (BJT) portfolios in the industry, and for good reason. The basis for small signal BJTs is simple; they are the best way to amplify an input signal without introducing large amounts of distortion to the output signal, creating near ideal amplification. This is completed through the use of a quiescent point (Q-point), which is a point of conductance on the load line of BJTs. The Q-point represents the optimal DC biasing point for a given amplification topology, which occurs between saturation and cutoff. Biasing the device at the Q-point allows for the BJT to remain in the active region, fully capturing the amplifier's output without losing a portion of the signal to cutoff or saturation.

This not only makes small signal BJTs effective, but also extremely versatile. Since the output signal is an amplified reflection of the input signal, it is possible to layer multiple amplifiers and create a multi-stage system without introducing undesirable gain to distortions. This opens up the possibility to construct many circuit topologies, where each stage has a specific amplification function. Each individual stage is typically comprised using one of three popular configurations, which are called common base, common collector, and common emitter. While the function of each amplifier is different, they can all be represented using the hybrid- $\pi$  model. In this model, an impedance  $r_{\pi}$  is placed between the base & emitter terminals, and a dependent current source  $g_m V_{\pi}$  is placed between the collector & emitter terminals. The current source,  $g_m V_{\pi}$ , is representative of the small signal collector current, where  $V_{\pi}$  is the voltage drop across  $r_{\pi}$  and  $g_m$  is the transconductance of the device. It is important to note that both  $r_{\pi}$  and  $g_m$  are can be altered by modifying the DC current signals. Also included in the hybrid- $\pi$  model is the output resistance  $r_o$ , which is dependent on BJT early voltage. Pictured in **Figure 1** are the equations used for determining these parameters.

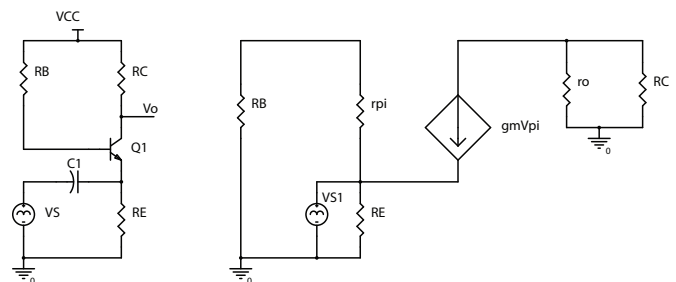
$$r_{\pi} = \frac{V_T}{I_B} \quad g_m = \frac{I_C}{V_T} \quad r_o = \frac{V_A + V_{CE}}{I_C}$$

**Figure 1:**  
Hybrid- $\pi$  BJT Parameters

### Common Base:

The common base structure is used to create a current follower amplifier with voltage gain. As the name implies, the base is tied to ground and is common to the input and output. The emitter is used for the input signal and the output is taken at the collector. Since the input-output relationship is represented by the emitter-collector, the amplifier is a current follower, as  $\frac{I_C}{I_E} \approx 1$ . This is convenient for design engineers who wish to achieve voltage amplification without modifying the current signal.

By performing circuit analysis on the hybrid- $\pi$  model, the expression for voltage gain can be derived. This expression reveals the key gain parameters for the common base structure, which are  $R_C$ ,  $R_B$ ,  $\beta$ , and  $r_{\pi}$ . This is demonstrated in **Figures 2 & 3**. The gain factor,  $\beta$ , can be controlled in transistor selection. Following that,  $R_C$  and  $R_B$ , can then be selected to yield a target  $r_{\pi}$  and ultimately the desired voltage gain. It is important to note that output resistance  $r_o$  is often much larger in scale than  $R_C$ . For this reason, it is fair to approximate the parallel relationship of  $R_C // r_o$  as  $R_C$ .



**Figure 2:**  
Common Base Amplifier

$$V_o = -g_m V_{\pi} (R_C // r_o)$$

$$V_{\pi} = -V_s \frac{r_{\pi}}{r_{\pi} + R_B}$$

$$A_V = \frac{g_m (R_C // r_o) r_{\pi}}{r_{\pi} + R_B} = \frac{\beta R_C}{r_{\pi} + R_B}$$

**Figure 3:**  
Common Base Voltage Gain



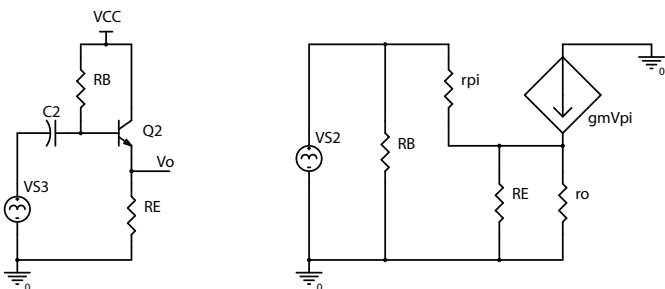
## Common Collector:

Opposite to the common base structure, the common collector structure is a voltage follower with current gain. The collector is tied to ground with the base used for the input signal. Output is taken at the emitter, which is also the location for output resistance  $r_o$ . Since base current represents the input current and emitter current represents the output current, current gain for the amplifier can be approximated as:

$$\frac{i_E}{i_B} \approx \frac{i_C}{i_B} = \frac{\beta}{1+j\omega(C_j+C_d)r_\pi} = h_{fe}$$

In this case,  $h_{fe}$  is small signal current gain versus frequency.

Confirmation of the common collector's voltage follower property can be achieved by performing circuit analysis in the same manner as the common base. When the expression for voltage gain is derived, it becomes evident that the numerator and denominator are the same, equating a 1-to-1 system. Just as with the common base amplifier,  $r_o$  will be significantly larger than  $R_E$ , thus  $r_o//R_E$  can be approximated as  $R_E$ . An example of the common collector amplifier and the associated voltage gain derivation are shown in **Figures 4 & 5**.



**Figure 4:**  
Common Collector Amplifier

$$V_o = g_m V_\pi (R_E // r_o)$$

$$V_s = V_\pi + g_m V_\pi (R_E // r_o)$$

$$A_V = \frac{g_m (R_E // r_o)}{1 + g_m (R_E // r_o)} \approx \frac{g_m R_E}{g_m R_E} = 1$$

**Figure 5:**  
Common Collector Voltage Gain

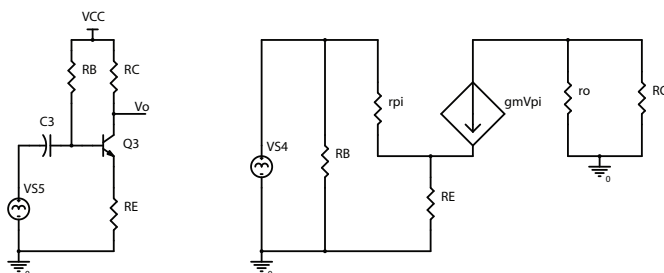
## Common Emitter:

The most popular small signal configuration is the common emitter configuration, which provides both voltage and current gain. The emitter is the common ground point, with the input signal applied to the base and the output signal taken at the collector. Since the output is taken at the collector, output resistance  $r_o$  is drawn in parallel with  $R_C$ , like common base implementation. Similar to common collector implementation, the small signal current gain can be written as:

$$\frac{i_C}{i_B} = \frac{\beta}{1+j\omega(C_j+C_d)r_\pi} = h_{fe}$$

Here, base current represents the input current and collector current represents the output current.

The voltage gain of the common emitter can be approximated with the expression  $\frac{R_C}{R_E}$ , giving the design engineer total control over the voltage gain in the system. This expression is ultimately realized through hybrid- $\pi$  model circuit analysis, just as with the common base and collector configurations. As with the other amplifier configurations, output resistance  $r_o$  can be neglected if it is significantly larger than  $R_C$ . An example of a common emitter amplifier and the derivation for the associated voltage gain can be seen in **Figures 6 & 7**.



**Figure 6:**  
Common Emitter Amplifier

$$V_o = -g_m V_\pi (R_C // r_o)$$

$$V_s = V_\pi + g_m V_\pi R_E$$

$$A_V = -\frac{g_m (R_C // r_o)}{1 + g_m R_E} \approx -\frac{g_m R_C}{g_m R_E} = -\frac{R_C}{R_E}$$

**Figure 7:**  
Common Emitter Voltage Gain

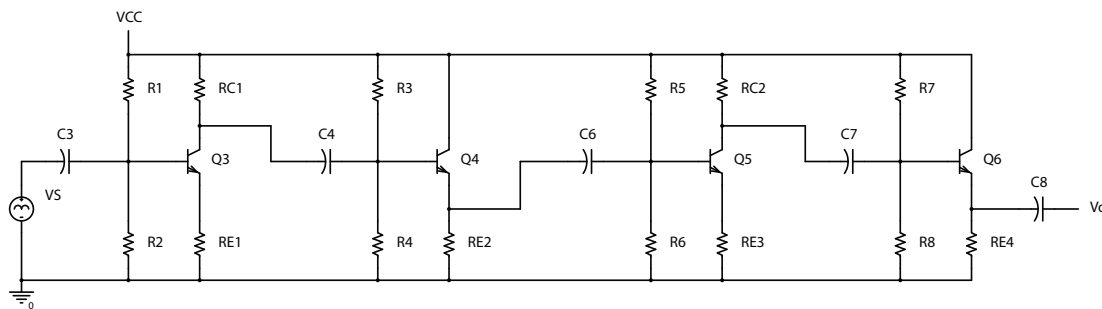
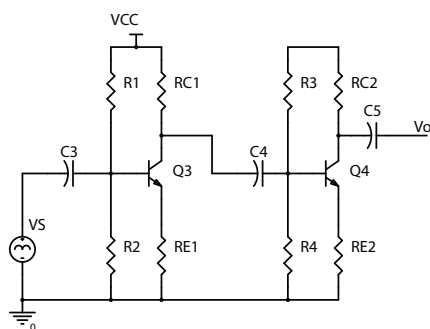


## Multi-Stage Amplifiers:

The small signal amplifier stages discussed are most effective when implemented in multi-stage amplifiers. A popular example of this is the cascade common emitter amplifier. In this device format, common emitter amplifiers are coupled to provide pairs of gain stages. By implementing the stages in pairs, it is ensured that the overall system gain isn't inverted from the original signal. If signal inversion is desired, an odd number of amplifier stages can be used. It is important to implement coupling capacitors in this type of amplifier. Coupling capacitors do not affect the AC signal, but can block the DC signal. This allows design engineers to operate each BJT in the system at its respective Q-point. In **Figure 8** below, Central Semiconductor's CMPT6428 (Q3 & Q4) is used to implement a two-stage cascade common emitter amplifier.

An improved version of this amplifier couples a common emitter amplifier with a common collector amplifier. The benefit of implementing a system like this is the common collector's low output impedance, which reduces signal attenuation. The common emitter provides the gain and the common collector acts as a low output impedance voltage follower, yielding a near ideal voltage source with gain. Then, each common emitter-collector pair is cascaded with another common emitter-collector pair, which forms the full multi-stage amplifier. In **Figure 9** below, Central's CMPT6428 (Q3 & Q5) and CMPT3904 (Q4 & Q6) are used to implement a four-stage cascade common emitter-collector amplifier.

**Figure 8:**  
Common Emitter  
Cascade Amplifier



**Figure 9:**  
Common Emitter-Collector Cascade Amplifier

## Conclusion:

As demonstrated throughout this publication, small signal BJTs are extremely practical and adaptable. They can be implemented in a variety of ways to form a multitude of different amplifier topologies, ranging from simple buffers to more complex multi-stage sources with gain. Including the CMPT6428 and CMPT3904 used in the figures above, Central Semiconductor currently has more than 900 different small signal BJT options in its product portfolio. The large selection of small signal BJT products Central manufactures allows design engineers to select and implement the exact BJTs needed to satisfy any small signal amplification requirements.





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145 Adams Avenue  
Hauppauge, NY 11788, USA  
1.631.435.1110  
[www.centalsemi.com](http://www.centalsemi.com)

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